ATCA platform certification for NSW Trigger Processor

- Preliminary -

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# General

In general terms, all necessary i/o data paths must be tested and verified in hardware. This includes all data paths for ancillary functions, TTC, monitoring, etc., as well as optical i/o for interfacing to detector data collectors and sector logic[[1]](#footnote-1). On the other hand, with the exception of the main trigger processing algorithm, it is not necessary that all functions performed in firmware need to be tested and verified in hardware. In many cases, it will be sufficient to estimate the resources required for some functionality in order to verify that the FPGA resources are sufficient. If it appears that the FPGA resources will come close to being fully utilized, then detailed implementation must be done.

# Hardware requirements

The following hardware requirements are based on diagram in Appendix A of Sorin’s document “High Density Optical Receiver Mezzanine Board for ATCA-SRS. Specifically, that document calls for a “Rear Transition Module” to receive TTC and other information from FELIX and transmit it to the ATCA carrier cards where it is decoded and sent to the Mezzanine Cards. Using this path, as opposed to connecting TTC directly to optical receivers of AMC card has the advantage that it need only be done once per ATCA blade as opposed to having it done on eight separate FPGAs on Mezzanines. Doing so relieves those FPGAs of that function so that its resources can be fully dedicated to the task of implementing the trigger algorithms. Also, the monitoring functions, if implemented in the carrier, can take advantage of the carrier’s SDRAM to buffer large amounts of data.

>> SRS Carrier was tested with 2GByte SO-DIMM DDR3 RAM

>> RTM SFP connections are typically being used for 1Gb Ethernet or 10GbEthernet (XAUI). Will test them to the limit of carrier FPGA (5-6Gbps)

## Powered ATCA Crate – Details ??

## Shelf Manager - ??

## Rear Transition Module - ??

## External Ethernet Switch - ??

## ATCA based Ethernet Switch - ??[[2]](#footnote-2)

## FELIX or FELIX Emulator (Xilinx eval board) - ??

## AMC Optical Front End Emulator (Xilinx Eval Board) - ??

## Anything else - ??

# Hardware tests

These tests are listed in order from lowest level to highest level in terms of functionality. All described functionality must be fully tested and verified.

## Smoke test -

Power up test to insure all power supply voltages on Carrier and Mezzanine are correct. Power supply currents should be measured.

## IPMC / MMC management and monitoring.

>> Our team will focus on implementing the specific panel development in ATLAS DCS System (WinCC) fwATCA framework. Until that is being done, web-based shelf-manager communication may be used instead.

>> IPMC / MMC can perform power-up/down, FPGA reboot, carrier and mezzanine sensor readout, FPGA IPMI extension (access to Virtex-7 XADC/Sys Monitor for temperature and internal voltage sensing, access to microPods I2C sensors, etc. – pending firmware implementation)

## Clock network / Jitter-cleaner.

>> The mezzanine has 6 PLLs in total with 4/6 outputs. Unfortunately there are no test connectors; clock signals may be routed to the mezzanine interface and picked up there with some signal degradation. Ultimately, the GTH link stability will be an indirect measure of the clock quality.

>> One interesting case would be the clock recovery from one of the optical links and local cleaning through the PLLs. GBT firmware implementation will be needed for this together with an external GBT source. For clock tests only, perhaps a “light” GBT implementation with only serdes (no protocol) would suffice.

## FPGA Configuration

FPGA configuration is done through the IPMC in the Shelf Manager. The Carrier decodes this information and produces a JTAG stream to configure the Carrier’s FPGA. The Carrier then passes JTAG configuration data to the FPGAs on the Mezzanine cards.

>> On the SRS carrier, the JTAG passes through a small (Spartan6) FPGA which is connected to the carrier IPMC, as well as the two carrier FPGAs, therefore JTAG configuration can be performed either via IPMC (via Base Ethernet link) or via an RTM Ethernet connection (bypassing IPMC). In both cases, firmware and software need to be developed.

>> For initial tests and benchtop operation, the mezzanine has a dedicated JTAG connection

Verify the FPGA configuration BPI flash is operational.

## Verify operation of the carrier SDRAM

>> SRS Carrier was tested with 2GByte SO-DIMM DDR3 RAM

## General purpose i/o

### Carrier LVDS(52) and GTx(4) through full mesh backplane

### Carrier GTH(16) through RTM per carrier

### Check Carrier to Mezzanine general purpose i/o in both directions – LVDS(50), GTH(8) per mezzanine

## Ethernet monitoring

### Full Mesh Backplane

Write and read back test monitoring data through ATCA switch and backplane to Carrier cards. Verify data path up to Mezzanines.

>> IBERT tests on the backplane links at the required speed or higher would be a minimal test. Protocol implementation I guess is part of the ancillary functions task.

### Rear Transition Module

Write and read back test data through Rear Transition Module to Carrier Cards. Verify data path up to Mezzanines.

>> RTM SFP connections are typically being used for 1Gb Ethernet or 10GbEthernet (XAUI). Will re-test them (IBERT) to the limit of carrier FPGA (5-6Gbps)

## TTC

### Rear Transition Module

TTC data sent by FELIX (or its emulator) via GBT should be sent through RTM to Carrier. Carrier FPGA must decode TTC data and send it to Mezzanines where it must also be verified.

>> as for 3.3, “light” GBT implementation with only 4.8Gbs serdes can be used for validating clock recovery scheme.

## Optical i/o

SRC Mezzanines contain 36 channels each of optical receivers and transmitters. These may be tested, for example, by looping outputs back to inputs and doing BERR testing on all 36 channels. Trigger algorithms are not needed for this test.

>> Optical links will be tested (a) at highest possible speed (i.e 10.3Gbps) and (b) at a mixed speed configuration emulating the use in experiment (32 downlinks at 4.8/5.5-6 Gbps (MM/sTGC case), 14 uplinks at 6.4 Gbps(?) (Sector Logic) and 4 duplex 4.8Gbps (FELIX)). In case (b) the two FPGA will be configured with opposite polarity.

>> BER threshold?

## Lateral LVDS(64) and GTH(8)

These must be functionally tested by transmitting from one of AMCs FPGAs and receiving on the other. These should be checked in both directions and their data rate vs BERR should be measured. Maximum bit rate per LVDS line should be established.

>> BER threshold?

## ATCA monitoring functions

# Functional testing

## Trigger Algorithms

Download sTGC and Micromegas Trigger Algorithms to Mezzanine FPGAs. Firmware need not be “finalized” so long as we have confidence that full algorithms “fit” into the resources of the FPGAs. Algorithms, or simplified ones, may be tested using simulated data sent by Ethernet links. Algorithms should also be tested on simulated data carried by optical inputs.

>> full trigger algorithm implementation is not the scope of the initial board test. However, emulating the power consumption of the final application, as realistic as possible, is an interesting case from the point of view of heat dissipation and power supply stress.

### Optical outputs to Sector Logic

Monitor optical outputs to verify trigger candidates are being sent correctly to Sector Logic from both MM and [[3]](#footnote-3)sTGC sections.

### Lateral LVDS (trigger candidates)

Send test “packets” in established trigger candidate format from MM FPGA to sTGC FPGA. Check and compared with data received on sTGC FPGA.

1. [↑](#footnote-ref-1)
2. [↑](#footnote-ref-2)
3. [↑](#footnote-ref-3)